Revving up VPX for 10Gbaud operation – a case study for implementing IEEE 802.3ap 10GBASE-KR over a VPX backplane

Bob Sullivan, Michael Rose, Jason Boh

Introduction
VPX has become the defacto standard for the current generation of military embedded computing platforms. These systems include high-speed serial fabrics such as Serial Rapid I/O, PCI Express, or Ethernet.

The initial VPX standards have focused on Gen1 Serial RapidIO, Gen 1 PCIe, and XAUI with maximum baud rates of 2.5 to 3.125Gbaud, Even supporting these rates is not a simple task often requiring a detailed signal integrity analysis and careful attention to the overall loss budget and the numerous signal impairments to insure success first time out. The new VITA 65 OpenVPX standard plans to add options for 5 and 6.25Gbaud as well in order to support Gen2 Serial RapidIO and Gen 2 PCIe.

The recent adoption of IEEE 802.3ap 10GBASE-KR, and the availability of silicon transceiver devices from a number of silicon vendors including AMCC, Broadcom, and Xilinx, provides the basis for the next increment in VPX performance. This is the first standard communication protocol to support 10gbaud per pair operation over a backplane so it is a natural next step for VPX to implement 10GBASE-KR for rugged applications. 10GBASE-KR will require a signal integrity analysis paradigm shift from the classic time domain approaches (e.g. eye diagrams) to frequency domain and statistical approaches. Gen2 Serial RapidIO and Gen 2 PCIe include some of this thinking, but 10GBASE-KR takes it to a whole new level.

Designing a compliant inter-operable channel for 10.3Gbaud over a single lane on a typical VPX backplane poses a number of technical challenges. This paper evaluates a representative VPX channel for 10GBase-KR compatibility using the IEEE 802.3ap compliance metrics. The tools and techniques for simulating a 10Gbaud channel will be discussed.

VPX Channel Topology
Vita 46 systems come in a number of mechanical form factors. Regardless of the chassis arrangement, VPX backplanes are implemented in either 3U or 6U heights. The VPX REDI standards detail the slot pitch (0.8”, 0.85”, 1.0”), the connector footprint, and the pin assignments for differential pairs. A representative channel topology is shown in Figure 1. Backplane traces can range from 1” for adjacent slots to about 17” for a 21-slot, 0.8” pitch system. Typically, the maximum trace length is limited to control the maximum attenuation. For this study, we will consider a maximum backplane trace length of 17”.

Revision 0.6
Revving up VPX for 10Gbaud operation – a case study for implementing IEEE 802.3ap 10GBASE-KR over a VPX backplane

Bob Sullivan, Michael Rose, Jason Boh

Figure 1 – VPX backplane simulation topology

VPX module trace lengths can range from roughly 1.5” with the transceiver placed just next to the connectors to a practical maximum of about 4”. In terms of the frequency-dependent skin-effect losses, the module’s trace length will often have more impact on the overall channel attenuation than the backplane traces because of the small etch geometries typically used on module PCBs. For this study, we assume that the module does not include a mezzanine connector/PCB in this path.

10GBase-KR Compliant channel
The IEEE 802.3ap specification defines a compliant channel with specific test point locations. The test channel does not include the transceiver package impairments or the discontinuities related to the BGA escape via or AC coupling capacitors. The test points which define a test channel are noted as TP1 to TP4 in the VPX backplane simulation topology diagram shown in Figure 2.

The 10GBase-KR specifies a number of frequency domain parameters in Annex 69B that can be used to evaluate channel conformance such as fitted attenuation, insertion loss deviation, return loss, and insertion loss to crosstalk ratio. The transmit and receive blocks have their own compliance metrics which are not simulated or discussed in any detail in the paper. The benefit of a compliant channel is that link performance can be evaluated with the assumption that the transceivers are known to be compliant. This study focuses exclusively on the VPX channel and will use behavioral transceivers integrated into the ADS channel simulation environment to replicate 10GBase-KR transmitter and receiver characteristics.

PCB Trace Topology for Simulation
For simulation, the channel topology in Figure 2 below was constructed as a 6-port mixed-mode cascaded model of the trace sections, the VPX connectors, and their corresponding footprint vias.
The trace sections were constructed with ADS’s lossy 2D multi-layer transmission line models which model dispersion from frequency-dependent dielectric and skin-effect losses (the dielectrics are assumed to be homogeneous). The transmission lines are implemented as symmetrical striplines arranged as 3 co-planar pairs. Pair-to-pair separation was set to be 3 times the trace-to-plane dielectric height. This value allows realistic routing rules but will tend to overestimate crosstalk from adjacent trace coupling. (Note that FEXT is largely mitigated in stripline topologies.) The center victim pair is assumed to be an RX path and the outer pairs are configured as near-end or far end TX pairs for worst-case NEXT crosstalk simulations. In real world implementations, the backplane will generally permit much more generous pair-to-pair spacing rules and some attention is usually given to separate TX and RX pairs.

Each pair in the channel model is assigned a mixed-mode port as shown in Figure 2. An ideal 100Ω differential termination is applied to each port for the frequency-domain analyses (as a result, the simulations will underestimate the effects of real world trace and termination impedance discontinuities).

**VPX Connector Modeling**

VPX systems based on VITA 46 utilize a MultiGig-RT2 connector; this represents the vast majority of systems in use today. Recently, an alternative Viper connector has become available as well (VITA 60 draft) but it is not in widespread use today. Since the connectors share the same via footprints and pinouts, we will study both of these connectors.

The 3-pair VPX connector model used primarily in the paper was developed by the vendor using a full-wave EM modeler/solver. Pin assignments for VPX connectors are defined in the corresponding Vita 46 “dot” specification. The current Vita 46.x specification uses a common pin arrangement for differential pairs among all the fabric variants. A section of a differential VPX connector with the standard pin assignments is shown in Figure 3. The shaded portion of the connector diagram represents the section characterized in the connector S-parameter model.
Revving up VPX for 10Gbaud operation – a case study for implementing IEEE 802.3ap 10GBASE-KR over a VPX backplane

Bob Sullivan, Michael Rose, Jason Boh

Figure 3 – VPX connector footprint

The fully-coupled 3-pair via models were developed in a full-wave EM solver. Three via cases were developed to evaluate the impact of overall via length and stub length.

Figure 4 – VPX footprint 3D via model

The backplane and module connector footprint vias were constructed with different stack-ups to represent PCB constructions generally found in VPX systems. Both PCB stack-ups are composed of 8 stripline layers and 4 plane pairs. All stripline signal layers are referenced to ground planes on both top and bottom to reduce power plane noise coupling at the via transitions. The overall thickness of the backplane PCB is 175mils and the module thickness is 115mils. A stripline section is shown below in Figure 5 along with the trace geometries used in the simulation. The dimensions shown are in mils.

Figure 5 – VPX simulation stack-up

The footprint via simulation models include optimized via geometries.

The via models use a “submerged coax” interface to emulate the signal launch from the buried press-fit connector pin. The coax shield is terminated to the grounding vias with a layer of perfect conductor. Non-functional pads are removed leaving a total of 3 pads per via (top, bottom, and trace escape). The model includes a
parameter for setting the back-drilling depth to configure the via stub length. In the back-drilled cases, there are effectively only 2 pads per via.

Figure 6 – Via model cross-section (short via case shown)

Simulation Methodology
The cascaded channel models are swept in the frequency domain in ADS and the behavior is plotted against the limits established in Annex 69B of the IEEE 802.3ap specification. The Annex 69B post-processing equations and limit expressions are implemented directly in ADS. The channel frequency domain model is also converted to time-domain to gain some insights as to the relative impedance discontinuity magnitudes.

Statistical techniques are used to evaluate eye contour opening and to generate horizontal and vertical bathtub curves. A statistical domain analyses provides a fast and accurate method for evaluating operating margins and for tuning equalization parameters. The number of bits needed to accurately predict eye opening margins using conventional transient, time-domain process can be determined by comparing the settling time of the channel’s pulse response. Often the settling time will be a factor of 20 or more relative to the bit time, requiring a transient analysis period of $2^{20}$ or $10^6$ bit times.

Statistical analysis techniques use the channel’s time domain pulse response to build a cumulative distribution function from horizontal and vertical probability density functions. Random jitter is added to the horizontal PDF as well as any crosstalk noise sources. ADS builds on the methodology developed in StateyeRef 1 adding proprietary algorithms for accurate handling of jitter effects (RJ, PJ, and DCD). The channel must be linear and time invariant to guarantee accurate results.

Bit encoding is not used in statistical analysis. The pattern dependent effects of 64b/66b encoding used in 10GBase-KR can be evaluated with ADS’s bit-by-bit simulation technique which uses superposition of the channel’s step response. Both rising and falling edges are used for jitter modulation.

The simulations performed in this study do not include the effects of manufacturing tolerances such as dielectric dispersions, trace or termination impedance variations or conductor roughness. Also, environmental variations are not considered. Generally, these effects can impact margins by as much as 20 percent.
Discontinuities related to trace impedance variations can increase passband ripple in the frequency domain and ISI in the eye contour simulations.

**VPX Connector Simulation**

Naturally, the largest impedance discontinuity feature of a conventional VPX channel is the connector and its footprint through vias. Dispersions within the connector create crosstalk and mode conversions. VPX backplane connectors have a 1.8mm pitch which, along with a fairly large footprint via barrel diameter, will typically result in characteristic differential impedance as low as 85Ω. The contact patch for the press-fit connector pin extends 20-30 mils into the top of the via creating an intrinsic top stub. The length tolerance of the connector pin contact zone effectively limits the depth of back drilling (or blind or stepped via length) and precludes top drilling.

![VPX connector](image)

**Figure 7 – VPX Connector pin/via detail**

Further complicating stub length management for some applications, VPX mid planes conforming to Vita 46.10 has an additional constraint: a requirement that the overall thickness of the PCB should be .212” nominal.

Adverse effects arising from the backplane via stubs can mitigated to some degree by limiting layer assignments, by back-drilling the stubs, and by optimizing anti-pad geometry. However, even in the best-case, the capacitive nature of the VPX connector footprint via will create a significant impedance drop. To meet 10GBase-KR bit error rate requirement, deep resonant nulls in the SDD21 behavior from the vias cannot occur within the signaling band.

To further understand the impact of the connector and its footprint vias, just the connector section of the channel was swept in the frequency domain and then converted to differential T-parameters in the ADS SP TDR tool. The 3 via length/stub cases were simulated for the C2:D2 pair. Note that of the 3 pairs in the connector model section, the C2:D2 pairs exhibited the largest absolute discontinuity.

The following VPX connector via cases shown in Table 1 were selected for evaluation because they allow routing on 6 of the eight available signal layers with a maximum of 2 levels of back-drilling. Note that in the low-volume, mission-critical VPX marketplace, the costs for back-drilling and low loss dielectric materials can generally be justified.
Revving up VPX for 10Gbaud operation – a case study for implementing IEEE 802.3ap 10GBASE-KR over a VPX backplane

Bob Sullivan, Michael Rose, Jason Boh

### Table 1 – Connector footprint via simulation cases

<table>
<thead>
<tr>
<th>Case</th>
<th>Backplane via length</th>
<th>Backplane stub length</th>
<th>Module via length</th>
<th>Module stub length</th>
</tr>
</thead>
<tbody>
<tr>
<td>Long via / long stub (LVLS)</td>
<td>175</td>
<td>50</td>
<td>115</td>
<td>35</td>
</tr>
<tr>
<td>Long via / short stub (LVSS)</td>
<td>150</td>
<td>25</td>
<td>100</td>
<td>15</td>
</tr>
<tr>
<td>Short via / long stub (SVLS)</td>
<td>75</td>
<td>40</td>
<td>50</td>
<td>25</td>
</tr>
</tbody>
</table>

Figure 8 – Connector footprint via simulation cases

From the following differential TDD11 plots, the connector and footprint via discontinuities can be easily compared. Please note that some nominal Hamming windowing is applied to remove residual Nyquist ringing. Also a peeling algorithm, a unique feature in ADS, has been applied to improve accuracy for the far-end discontinuities.

In the first LVLS case (shown in Figure 9), the C2:D2 connector pin section discontinuity, while substantial, is small relative to the 20Ω drop of the backplane footprint via.

Figure 9 – TDR, LVLS case
Removing 25 mils from the long via stub reduces the via impedance delta to a value similar to that of the C2:D2 connector section. For long vias, this is a significant improvement and will improve the crosstalk performance and passband ripple for the channel.

**Figure 10 – TDR, LVSS case**

Short vias can tolerate the longer stub defined for this case, even providing improved performance compared to the LVSS case.

**Figure 11 – TDR, SVLS case**

If we substitute the electrically shorter A1:B1 connector pair in the SVLS case, we can see the performance degrade slightly because of the relative impedance “bias” seen at the connector-to-module via transitions resulting in a greater absolute impedance discontinuity (approximately 83Ω).
The impact of these 3 via cases on the overall channel performance will be evaluated further in the following frequency domain and eye contour simulations.

**Channel Frequency Domain Behavior**
The good SDD21 and SDD11 performance of the overall channel reflects the attention paid to limiting stub length as well as the use of a low loss dielectric material. Differential insertion loss at the Nyquist frequency of 5.156GHz is in the range of -10.5dB and -13dB. The low overall channel attenuation allows designers to consider using less expensive dielectric materials. However, the additional signal-to-noise ratio afforded by the low loss material provides greater crosstalk margins as discussed in the following crosstalk section. This turns out to be an important consideration in meeting 10GBase-KR ICR (insertion loss to crosstalk ratio) limits. Also, the low overall differential insertion loss provides some flexibility for systems with longer trace lengths or more narrow trace widths.

Also important is the fact that there are no significant resonances in the forward channel behavior. Even the long via/long stub case demonstrates only moderate insertion loss deviation.
Figure 14 below shows return loss for the 3 via cases. While the LVLS case demonstrates roughly 4dB less differential return loss, the overall performance for all 3 via cases easily meets 10GBase-KR requirements.

![Graph showing return loss for 3 via cases.](image)

*Figure 14 – Channel frequency domain SDD11, 3 via cases*

Given the low passband ripple and the relatively low attenuation in the signaling band with the worst-case LVLS configuration, the following frequency domain analyses focus on this via scenario with the exception of the crosstalk evaluation where the via length has a considerable impact on ICR margins.

The forward loss characteristics of the worst-case channel are plotted against the 802.3ap Fitted Attenuation and Insertion Loss Deviation limits, and are well above compliance limits. There is considerable loss margin to help counteract the effects of environmental variations and manufacturing tolerances.

![Graph showing channel frequency domain fitted attenuation and insertion loss.](image)

*Figure 15 – Channel frequency domain fitted attenuation and insertion loss*

Insertion Loss Deviation is a clear indication of the channel’s passband ripple performance, which in turn is largely related to good connector/via discontinuity characteristics. This metric is an important indicator of the suitability of a particular connector system. With careful management of the connector footprint via and anti-pad, this VPX connector demonstrates surprisingly good performance at 10.3Gbaud. The second plot in Figure 16 is for the same section of a VPX connector from another vendor. While the peak ripple is slightly higher, the performance is comparable.
The channel also has good margin to the IEEE 802.3ap recommended return loss limits as shown in Figure 17.

**Frequency Domain Crosstalk Characteristics**

Note that in the VPX differential pair pinout, the C:D pair has two adjacent near end aggressors (E:F pairs) and 2 adjacent far end aggressors (A:B pairs), so it is a reasonable worst-case pair for crosstalk evaluation. The frequency domain differential NEXT and FEXT crosstalk performance was evaluated using 2 symmetrical, uncorrelated aggressor pairs acting on the C2:D2 pin pair. The power sums of the individual aggressors were calculated as specified in IEEE 802.3ap, Annex 69B. The PSFEXT and PSNEXT contributions were then power summed to form the overall crosstalk (PSXT).
As logic would dictate, the short via case (shown highlighted) displayed significantly lower NEXT and FEXT crosstalk levels than either of the long via cases. There was little difference between the 2 long via stub cases (shown, not highlighted). When combined as the total power sum crosstalk (PSXT), the overall crosstalk level is clearly lower in the SVLS case for most frequencies (as shown in Figure 19).

![Figure 19 – Channel PSXT, 3 via cases](image)

The architects of the IEEE 802.3ap specification did not define strict crosstalk limits. Instead, acknowledging that some less lossy channels could tolerate higher crosstalk levels, they defined a limit based on the ratio of insertion loss to the total crosstalk (ICR). This measure is analogous to Signal-to-Noise Ratio (SNR). Given the pitch and via barrel diameter of VPX connectors, this measurement method can be of particular benefit in VPX systems. As mentioned above, shorter vias tend to have substantially lower crosstalk. A system designer can trade off the costs of more expensive dielectric materials against a more restrictive routing policy where the 10.3Gbaud traces are routed exclusively on the top most layers.

In the test case, IEEE 802.3ap ICR limits are met with a low loss (dissipation factor of .0075@2.5GHz) dielectric material without introducing the layer routing restrictions mentioned above. The following ICR plots display the margins for the long via case (again, there is very little difference between the 2 long via stub cases) and short via case where the ICR margins are appreciably better.

![ICR plots](image)
Revving up VPX for 10Gbaud operation – a case study for implementing IEEE 802.3ap 10GBASE-KR over a VPX backplane

Bob Sullivan, Michael Rose, Jason Boh

Figure 20 – Channel ICR, 2 via length cases

Although we did not study this case, shorter backplanes may be able to utilize a higher loss dielectric, but the additional margin afforded by the low loss dielectric will likely be required to meet ICR limits for longer backplanes such as we studied here.

Statistical Eye Simulation

Since the VPX channel meets the IEEE 802.3ap Annex 69B compliance metrics, it should be able to support 10GBase-KR with the specified bit error rate.

As a proof point, the same 3-pair, worst-case channel topology described previously is now used to evaluate eye opening margins using various equalization adaptations. In the following section we compare the effect of the equalization settings on the SNR and eye contour vertical and horizontal opening height at the 802.3ap specified bit error rate (BER) of $10^{-12}$. The equalization scenarios are compared with no crosstalk and with 2 NEXT aggressors. The primary intent of the eye contour simulations is to understand the amount and proportion of equalization needed for a typical VPX channel.

The schematic used in the simulation is presented in Figure 21 (2 NEXT aggressors shown). The topology includes multi-pair, coupled IC package models for a representative IEEE 802.3ap transceiver.

Figure 21 – Eye contour simulation schematic

The transmitter is configured for a nominal output swing of +/-0.55V and a rise/fall time of 40pS. These values fall near the middle of IEEE 802.3ap minimum/maximum ranges respectively. (It is interesting to note that faster rise/fall times will generally yield better results in the equalized horizontal and vertical eye opening at the receiver but, at some point, the additional reflected energy returned to the driver will begin to degrade the link’s BER. Faster signal transition rates will also tend to increase crosstalk and EMI levels.)
Revving up VPX for 10Gbaud operation – a case study for implementing IEEE 802.3ap 10GBASE-KR over a VPX backplane

Bob Sullivan, Michael Rose, Jason Boh

A Random Jitter (RJ) value of 0.01UI_{\text{rms}} is applied to both the transmitter and the receiver. A Duty Cycle Distortion (DCD) value of 0.035UI is also applied at the transmitter to represent typical oscillator periodic jitter. The un-equalized receiver gain is unity. The crosstalk transmitters are configured identically as the through channel transmitter. The crosstalk transmitters have a random phase relationship and are uncorrelated. All transmitters are driven with a 31-bit Pseudo Random Bit Sequence (PRBS) stimulus.

10GBase-KR Equalization
IEEE 802.3ap specifies that transceivers implement, at minimum, 3-tap Feed Forward Equalization (FFE) in the transmitter and acknowledges the probable need for a multi-tap Decision Feedback Equalizer (DFE). Most 10GBase-KR transceivers will implement both FFE and DFE and will likely have a linear equalization stage in the receiver as well.

In order to establish reliable data exchange between link partners on startup the transmitter will send a specified training pattern at a reduced signaling rate. The receiver generates an error signal from the equalized training sequence and updates the transmitter tap coefficients in an iterative process converging on an optimized solution. ADS implements a similar adaptive FFE scheme in its behavioral receiver model using (among others) a Least Mean Squared (LMS) algorithm.

Generating a time domain Single Bit Response (SBR) provides some insights about the channel and an effective channel equalization strategy. From the SBR shown in Figure 22, several general conclusions might be drawn:

- The response takes approximately 20 bit times to settle implying that at least $10^6$ bits will need to be simulated for accurate results
- The low ripple in the tail of the response correlates to the low passband ripple observed in the frequency domain analyses
- Both pre-cursor and post-cursor equalizations are needed to optimize the channel’s SNR. Multiple FFE and/or DFE post-cursor taps will be needed.
- The response settles quickly indicating only a limited number of post-cursor DFE taps are needed to optimally equalize the channel.
Equalization Strategy
With 3 different equalization methods available in most 10GBase-KR transceivers, how is one chosen over another? The worst-case channel described in this paper could be generally characterized as having low attenuation, with low passband ripple, but with only marginal crosstalk immunity. Continuous Time Linear Equalization (CTLE) is not the best choice since the channel is not highly attenuated and linear equalization amplifies noise and crosstalk along with the signal. FFE is an appropriate choice since it provides both pre and post-cursor equalization. The number of taps implemented by silicon vendors will vary, but it is probably safe to assume that most will provide at least 2 pre-cursor and 2 post-cursor taps. Assuming a limited number of taps, FFE will probably not be able to “reach” the ripple out at the 4.5nS point in the SBR plot (Figure 22). DFE can provide the additional post-cursor equalization. The main draw back with DFE is that it, by nature, will tend to propagate bit errors, especially when the coefficients become large. 10G-Base-KR defines an optional Forward Error Correction (FEC) encoding sublayer for counteracting multi-bit burst errors. In addition, FEC can improve the effective BER performance of marginal channels.

The need for pre and post-cursor equalization is evident from the eye density diagram shown in Figure 23. With only 1 tap of pre-cursor and the main cursor 1 tap FFE equalization, there is no measurable eye opening.

Looking at Table 2, it is apparent that several taps of pre or post-cursor equalization is needed. With 2 taps of post-cursor, 2 pre-cursor taps yield a higher SNR but the effective eye opening is unchanged. As a general rule-of-thumb, achieving a BER of $10^{-12}$ or greater, an SNR of 17dB or more is needed (see below for an explanation on how SNR is computed). The test channel performs quite well with just 1 pre-cursor tap and 2 post-cursor taps of feed forward equalization.
In cases 5-8, multiple DFE taps are now added to the best FFE case. Increasing the number of DFE taps improves the margins progressively at least until the final, 4 DFE tap case. For the test channel, equalization case 7 provides the best performance.

### Table 2 – Channel FFE/DFE performance, no crosstalk

<table>
<thead>
<tr>
<th>Case</th>
<th>FFE Pre-cursor taps</th>
<th>FFE Post-cursor taps</th>
<th>DFE taps</th>
<th>SNR (dB)</th>
<th>Eye width @10^-12 (UI)</th>
<th>Eye height @10^-12 (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>-</td>
<td>16.89</td>
<td>.541</td>
<td>267</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>2</td>
<td>-</td>
<td>16.90</td>
<td>.536</td>
<td>267</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>1</td>
<td>-</td>
<td>18.21</td>
<td>.526</td>
<td>266</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>2</td>
<td>-</td>
<td>18.34</td>
<td>.526</td>
<td>265</td>
</tr>
<tr>
<td>5</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>18.43</td>
<td>.526</td>
<td>270</td>
</tr>
<tr>
<td>6</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>18.66</td>
<td>.531</td>
<td>278</td>
</tr>
<tr>
<td>7</td>
<td>2</td>
<td>2</td>
<td>3</td>
<td>18.98</td>
<td>.541</td>
<td>289</td>
</tr>
<tr>
<td>8</td>
<td>2</td>
<td>2</td>
<td>4</td>
<td>18.99</td>
<td>.540</td>
<td>289</td>
</tr>
</tbody>
</table>

Re-simulating the 8 cases described above with 2 NEXT aggressors, the channel exhibits slightly lower margins top-to-bottom, but is still well within the operating limits for a 10GBase-KR channel. The best FFE/DFE choice is highlighted.

### Table 3 – Channel FFE/DFE performance, 2 NEXT aggressors

<table>
<thead>
<tr>
<th>Case</th>
<th>FFE Pre-cursor taps</th>
<th>FFE Post-cursor taps</th>
<th>DFE taps</th>
<th>SNR (dB)</th>
<th>Eye width @10^-12 (UI)</th>
<th>Eye height @10^-12 (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1b</td>
<td>1</td>
<td>1</td>
<td>-</td>
<td>16.83</td>
<td>.531</td>
<td>256</td>
</tr>
<tr>
<td>2b</td>
<td>1</td>
<td>2</td>
<td>-</td>
<td>16.83</td>
<td>.536</td>
<td>256</td>
</tr>
<tr>
<td>3b</td>
<td>2</td>
<td>1</td>
<td>-</td>
<td>18.04</td>
<td>.516</td>
<td>256</td>
</tr>
<tr>
<td>4b</td>
<td>2</td>
<td>2</td>
<td>-</td>
<td>18.25</td>
<td>.516</td>
<td>256</td>
</tr>
<tr>
<td>5b</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>18.28</td>
<td>.521</td>
<td>262</td>
</tr>
<tr>
<td>6b</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>18.70</td>
<td>.531</td>
<td>274</td>
</tr>
<tr>
<td>7b</td>
<td>2</td>
<td>2</td>
<td>3</td>
<td>18.91</td>
<td>.536</td>
<td>284</td>
</tr>
</tbody>
</table>
Revving up VPX for 10Gbaud operation – a case study for implementing IEEE 802.3ap 10GBASE-KR over a VPX backplane
Bob Sullivan, Michael Rose, Jason Boh

<table>
<thead>
<tr>
<th>8b</th>
<th>2</th>
<th>2</th>
<th>4</th>
<th>18.93</th>
<th>.531</th>
<th>284</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 3 – Channel FFE/DFE performance, 2 NEXT crosstalk aggressors

The eye density and contour at BER $10^{-12}$ (inner-most opening outline) plots for case 7b is shown in Figure 25 and 26. The DFE transition responses are evident at zero-crossings. As mentioned earlier, faster rise/fall times will increase the SNR and horizontal opening (at the expense of crosstalk margins and power plane noise coupling). 10GBase-KR specifies a transition time of 24 to 47pS. At 40pS, the simulations were performed closer to the worst-case end of the allowable range.

![Figure 25 – Eye density and contour diagram, case 7b](image)

The horizontal and vertical bathtub plots display very good bit error rate margins up to and beyond $10^{-12}$ as shown in Figure 26.

![Figure 26 – Voltage and timing bathtub curves](image)

Conclusions

Although VPX is typically operated at 2.5 to 3.125 Gbaud today, the simulations performed indicate that VPX can support the IEEE 802.3ap 10GBase-KR 10.3Gbaud signaling speed. Advanced, adaptive equalization is the key to obtaining strong, reliable performance despite some inherent limitations of the VPX platform.

Mapping 10GBase-KR to VPX requires very careful attention to high-speed design details. The VPX topology simulated in this study is, not surprisingly, sensitive to crosstalk impairments but with careful attention to via tuning, it is fortunately free of large insertion loss ripple associated with connector-related impedance discontinuities. On more complex topologies, such as modules with transceivers...
Revving up VPX for 10Gbaud operation – a case study for implementing IEEE 802.3ap 10GBASE-KR over a VPX backplane

Bob Sullivan, Michael Rose, Jason Boh

located on a mezzanine card, designers will be faced with some difficult decisions regarding material selection, routing restrictions, spacing rules, trace geometries, and perhaps even connector pin assignments. Designers must pay particular attention to via impairments, both in terms of their overall length and their stub length.

System implementers must come to understand how to best apply equalization on a link-by-link basis. Fortunately, adaptive FFE and DFE equalization methods implemented in current 10GBase-KR transceivers will make this potentially complex task routine. We predict that 10.3Gbaud interfaces will become as common on Vita 46 platforms as 3.125Gbaud links are today. The VITA 68 group chaired by Bob Sullivan form Hybricon is currently working to define a VPX compliance channel to allow higher rates on VPX, initially aimed at Gen 2 SRIO and PCIe at 5 – 6.25 Gbaud, but with an eye toward 10GBase-KR as well.

References


Author Biographies

Bob Sullivan is the Vice President of Technology at Hybricon and is responsible for keeping abreast of industry technology trends, setting technical direction for the company, and defining technical approaches to solve challenging problems for Hybricon’s key customers. He is active on OpenVPX, VITA/VSO and PICMG technical standards committees, and he recently chaired the OpenVPX Development Chassis team. Mr. Sullivan has over 30 years’ experience in the design of high performance instrumentation and systems, holds a number of patents in the design of high performance systems, and has authored various technical papers and magazine articles.

Michael Rose has been involved in the design and development of analog and digital equipment for over 30 years. He has held numerous technical positions for companies such as NEC, Lucent, TI, and Avaya. In additional, Michael has operated a consulting practice for over 20 years, architecting and designing custom analog and digital devices including power devices & systems, embedded microprocessor boards, network processors and line cards, system management and protection devices. Michael specializes in high-speed system design and is an engineering consultant for Hybricon.

Jason Boh is an applications engineer for Agilent EESof EDA in the greater Boston area, where he is responsible for new product sales, customer training, and support. Jason holds a Master of Science in Electrical Engineering degree from the University of South Florida, where he participated in the Wireless and Microwave Information Systems (WAMI) program. His past experience includes design and fabrication of amplifiers, receivers, and other RF and microwave circuits using PCB, GaAs, and SiGe technologies. Jason also has expertise in high frequency test and measurement, high speed digital signal integrity simulation, electromagnetic simulation, and device modeling.